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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/023,170	02/13/98	HOLMAN T	042390.P5346

LM01/0808

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EXAMINER	
VERBRUGGE, K	
ART UNIT	**PAPER NUMBER**
2751	13

DATE MAILED: 08/08/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

See attached final office action.

LK

PTO-90C (Rev. 2/95)

1- File Copy

Office Action Summary	Application No. 09/023,170	Applicant(s) Holman
	Examiner Kevin Verbrugge	Group Art Unit 2751

☒ Responsive to communication(s) filed on *Mar 2, 2000*

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-20* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-20* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Response to Amendment

This final Office action is in response to amendment A, paper #10, filed 3/2/00. Claims 1-10 and 15-18 were amended. Claims 1-20 are pending. All rejections and objections not repeated below are withdrawn. Applicant's arguments have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 8, 9, 13, and 15-20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claims 1 and 17-20, Levy shows the claimed system memory controller as memory management unit 22 in Fig. 1, coupled

to memory bus 40. This system memory controller handles reads and writes as claimed.

Levy shows the claimed memory module as memory module 30 in Fig. 1. Memory module 30 includes the claimed plurality of memory devices as low stack 0-3 and high stack 0-3. Furthermore, memory module 30 includes the claimed memory module controller as memory transceiver 41 and memory control and timing unit 42. This controller receives a first memory transaction in a first format from the system memory controller and converts it into a second memory transaction in a second format for the plurality of memory devices as claimed. The second memory transaction is clearly different from the first memory format since the outputs of memory transceiver 41 and memory control and timing unit 42 are clearly different from their inputs. This is indicated by the differing nature of the signal lines shown in Fig. 1 and by the other figures and disclosure.

Regarding claim 2, Levy shows the claimed first memory bus as memory bus 40.

Regarding claim 3, Levy does not explicitly show the claimed clock signal line, however his control lines (indicated with "C" in Fig. 1) inherently include such a clock signal line since it

is essential for the processor system to be able to regulate its associated memory module(s).

Regarding claim 4, Levy does not explicitly mention the claimed handshake signal line, however it is inherent in his device since his memory controller necessarily communicates data to the system memory controller (memory management unit 22). It is clear that the memory module controller communicates data and control signals to the system memory controller since the data (D) and control (C) lines of memory bus 40 are bidirectional.

Regarding claim 5, Levy shows the claimed second memory bus as the signal lines coming out of memory transceiver 41 and memory control and timing unit 42.

Regarding claim 6, Levy's second memory bus includes the claimed signal line for a clock signal (timing signal) as shown in Fig. 1.

Regarding claim 8, Levy's memory buses clearly have different numbers of signal lines as shown by Fig. 1.

Regarding claim 9, Levy shows the claimed request handling circuitry as memory transceiver 41 and shows the claimed control logic as memory control and timing unit 42.

Regarding claim 13, Levy teaches that his memory devices are volatile, as claimed, since they are traditional random access memory devices.

Regarding claim 15, Levy shows a second memory module 31 in Fig. 1 which contains the claimed second plurality of memory devices and a second memory module controller as claimed.

Regarding claim 16, since the second plurality of memory devices refer to different memory addresses than the first plurality of memory devices, they store data in a different way than the first plurality of memory devices.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior

> art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7, 10, 11, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claim 7, Levy does not teach that his memory buses operate at different rates, however it would have been obvious to one skilled in the art at the time of the invention to operate them at different rates since they carry different signals and have different lengths, virtually ensuring that the maximum data rate of each one would be different.

Regarding claim 10, Levy shows separate address and data lines for both his first and second memory buses. He does not teach that his first memory bus carries time-multiplexed data and address information as claimed, however it would have been obvious to one skilled in the art to time-multiplex the first address bus to save signal lines and their associated cost and space.

Regarding claims 11, 12, and 14, Levy does not teach that his memory modules have the claimed characteristics, however it would have been obvious to the skilled artisan at the time of the invention to implement Levy's memory modules as SIMMs, DIMMs, or nonvolatile memory devices, as appropriate, depending on design considerations, since all three types of devices were well-known to the artisan.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of copending Application No.

09/023172 and claims 1-17 of copending Application No. 09/023234. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reasons.

Claims 1-20 of 09/023170 are directed to a memory module having memory devices and a memory module controller. A system memory controller is connected to the memory module controller with a memory bus.

Claims 1-14 of 09/023172 are directed to a memory module having memory devices and a memory module controller. A system memory controller (or a system memory module) is connected to the memory module controller with a memory bus. The memory module controller comprises interface circuitry to receive transactions from the memory bus and further comprises control logic to generate other transactions for the memory devices.

The memory module controller of 09/023170 necessarily includes interface circuitry to receive transactions from the memory bus and further necessarily includes control logic to generate other transactions for the memory devices, therefore 09/023170 is not patentably distinct from 09/023172.

Claims 1-17 of 09/023234 are directed to a memory module having memory devices and a memory module controller.

The memory module of 09/023234 is necessarily connected to a system memory controller of some sort (a special chip or the CPU) with a memory bus, therefore 09/023170 is not patentably distinct from 09/023234.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing

date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The method claims are grouped and rejected with the apparatus claims because the steps of the method are met by the disclosure of the apparatus and methods of the reference(s) as discussed above.

Any inquiry concerning this or an earlier communication from the Examiner should be directed to Kevin Verbrugge by phone at (703) 308-6663.

Any response to this action should be mailed to Box AF, Commissioner of Patents and Trademarks, Washington, D.C. 20231 or faxed to (703) 308-9051 or -9052 and labeled "OFFICIAL" or "UNOFFICIAL" as appropriate. Hand-delivered responses should be brought to Crystal Park 2, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Kevin Verbrugge

Patent Examiner

August 1, 2000

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